REMARKS

Claims 1-6 and 8-11 are pending in the present application. Reconsideration and allowance of pending claims 1-6 and 8-11 in view of the following remarks are requested.

The Examiner has rejected claims 1-6 and 8-11 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,834,355 to Brian S. Doyle ("Doyle") in further view of U.S. patent number 6,489,206 to Chen et al. ("Chen"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 5, and 10, is patentably distinguishable over Doyle and Chen, singly or in combination.

The present invention, as defined by independent claim 1, teaches, among other things, performing a source/drain extension implant, performing epitaxy to form raised source/drain regions, forming a silicide on the gate and source/drain regions, removing a spacer, thereby forming a void region between the source/drain regions and a gate, and performing a halo implant through the void. As disclosed in the present application, a implanted shallow source/drain junctions are formed between spacers and isolation trenches and raised source/drain regions are formed by epitaxy over the implanted shallow source/drain junctions. As disclosed in the present application, the spacers are then removed to create a void between the gate and the raised source/drain regions, and halo implant is performed through the void to form a halo around the gate in the channel region, which has a gate-defined length of approximately 50 nm or less.

As a result, the present invention achieves a highly localized halo implant in the channel region but not in the source/drain regions, which enables the present invention to advantageously achieve an improved channel doping profile in a MOSFET having a gate-defined channel length of approximately 50 nm or less. As a result, the present invention advantageously achieves a MOSFET having increased operating speed. Furthermore, the present invention achieves improved device density on a chip, which advantageously enhances manufacturing precision and efficiency.

In contrast to the present invention as defined by independent claim 1, Doyle does not teach, disclose, or suggest performing a source/drain extension implant, performing epitaxy to form raised source/drain regions, forming a silicide on the gate and source/drain regions, removing a spacer, thereby forming a void region between the source/drain regions and a gate, and performing a halo implant through the void. Doyle specifically discloses removing spacers 30, forming photoresist layer 70 over deep junction areas of both source region 40 and drain region 50, and then implanting halo structures 60 into the shallow junction areas of source region 40 and drain region 50. See, for example, column 2, lines 55-63 and Figures 1g, 1n, and 1o of Doyle. However, Doyle fails to teach, disclose, or suggest forming raised source/drain regions, forming a silicide on the gate and source/drain regions, removing spacers to form a void between the raised source/drain regions and the gate, and performing a halo implant through the void. Furthermore, Doyle provides no motivation for forming raised source/drain regions, removing spacers to form a void between the raised source/drain regions and the

gate, and performing a halo implant through the void. Moreover, Doyle fails to teach, disclose, or suggest a MOSFET having a gate defined channel region having a length of no more than 50 nm.

In contrast to the present invention as defined by independent claim 1, Chen does not teach, disclose, or suggest performing a source/drain extension implant, performing epitaxy to form raised source/drain regions, forming a silicide on the gate and source/drain regions, removing a spacer, thereby forming a void region between the source/drain regions and a gate, and performing a halo implant through the void. Chen specifically discloses forming raised source/drains 206 upward on substrate 200, removing sidewall spacers 205, forming lightly doped diffusion region 207 in the substrate between gate electrode 203 and raised source/drains 206, and performing a halo implant between raised source/drains 206 and gate electrode 203. See, for example, column 3, lines 15-39 and Figures 2B, 2C, and 2D.

Thus, in Chen, lightly doped diffusion region 207 is formed after raised source/drains 206 have been formed. As a result, raised source/drains 206 are not formed over lightly doped diffusion region 207. Furthermore, lightly doped diffusion region 207 does not extend between isolation regions and the gate. As a result, in Chen, the halo underlies all of lightly doped diffusion region 207. In contrast, the method disclosed in independent claim 1 results in a halo that underlies only a portion of source/drain extensions. Additionally, in Chen, a silicide is not formed on the gate and source/drain regions prior to removal of sidewall spacers 205, as specified in independent claim 1.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Doyle and Chen, singly or in combination. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Doyle and Chen. Thus claims 2-4 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Doyle and Chen for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 5, requires performing a vertical source/drain extension implant to a depth of approximately 10 nm to approximately 30 nm. Moreover, the present invention, as defined by independent claim 10, requires performing an approximately vertical source/drain extension implant in a region from the isolation trench to the gate, to a depth of approximatley 10 nm to approximately 30 nm. Also, independent claims 5 and 10 specify a similar sequence of steps as independent claim 1 discussed above. As such, and based on the foregoing reasons, both independent claims 5 and 10 are patentably distinguishable over Doyle and Chen. Thus, claims 6, 8, and 9 depending from independent claim 5 and claim 11 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Doyle and Chen for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 5, and 10 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-6 and 8-10 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-6 and 8-10 pending in the present application is respectfully requested.

Respectfully Submitted,
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